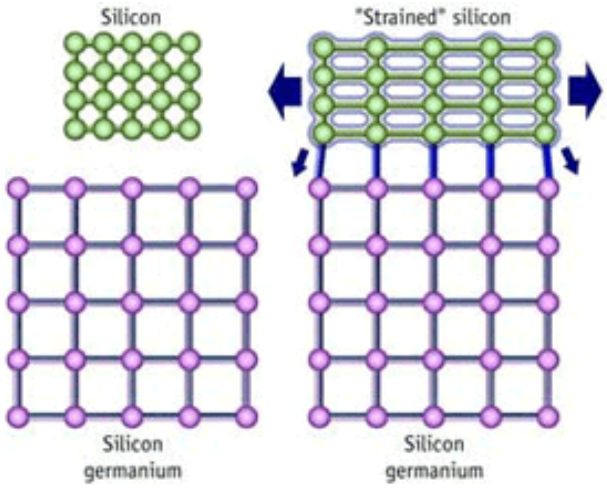
Strained Silicon

I. Basic Theory

- **Definition**
  - Strained silicon is a layer of silicon in which the silicon atoms are stretched beyond their normal interatomic distance.

- **Process**
  - Straining silicon can be accomplished by putting the layer of silicon over a substrate of silicon germanium.
  - As the atoms in the silicon layer align with the atoms of the underlying silicon germanium layer (which are arranged a little farther apart, with respect to those of a bulk silicon crystal), the links between the silicon atoms become stretched - thereby leading to strained silicon.
  - Stretching these silicon atoms reduces the atomic forces that interfere with the movement of electrons through the transistors.

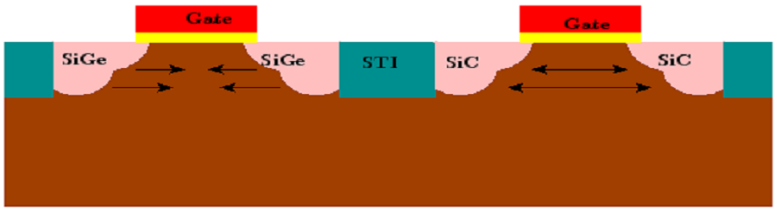
- **Benefits**
  - Increase Carrier Mobility.
  - Better chip performance.
  - Lower energy consumption.
  - Transistors switch 35% faster.
  - Increased drive current.



II. Local Strain Techniques

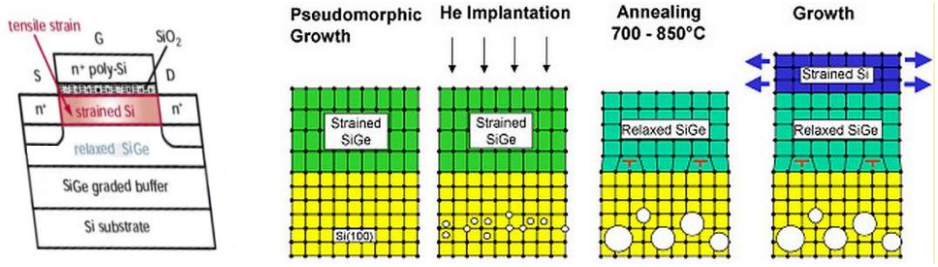
- **Contact Layers**
  - Strain is introduced into the channel through stressed contact layers.
  - It is grown using chemical vapor deposition techniques.
  - Compressive and tensile stress are required to enhance the performance of CMOS transistors
    - Compressive for PMOS.
    - Tensile for NMOS

- **Embedded Stressors**
  - This technique requires etching two cavities into Si, followed by epitaxially growing SiGe into the source and drain regions of the P-MOS devices, resulting in a compressive stress in the channel, which results in an improved hole mobility.
  - Similar mobility enhancements can be obtained for electrons by introducing tensile stress into the N-MOS channel by using SiC for the source and drain regions.

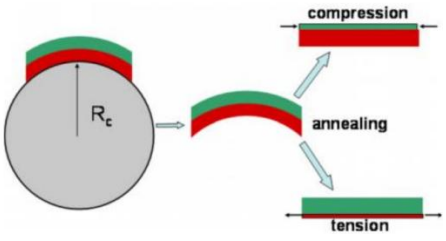


III. Global Strain

1. Biaxial Strain
   - Strains the X and Y directions.
   - Epitaxially grown SiGe layers on Si bulk wafers are used as substrate for strained silicon.
   - Threading Dislocations causes deterioration in device performance.
   - Methods to reduce threading dislocation defect density:
     - Relaxed SiGe buffer is grown on a graded SiGe layer.
     - The relaxation of a thin pseudomorphic SiGe layer using helium implementation.



2. Uniaxial Strain
   - Two wafers were bent over a cylinder creating a curved wafer with a strained state induced.
   - The curved wafers are brought into contact via direct wafer bonding and covalent bonds.
   - Splitting thin strained layers were transferred using hydrogen-induced layer.
   - The process can produce either tensile or compressive strain.
   - Strain values between about 0.08% and 0.04% were obtained for a radius of curvature ranging from 0.5 m up to 1 m.



IV. Strained Silicon Challenges

- Increased Junction Capacitance and Leakage, due to:
  - Higher Dielectric Constant and Lower Band Gap.
- Reduced thermal conductivity of SiGe, due to:
  - Increase in surface roughness.
  - Defects formation at the interface.
- Dislocation
  - The involvement of dislocations in these processes poses challenges for device application, such as control of leakage current and device yield.

V. Strained silicon on insulator (SSOI)

- We can combine the benefits of increase carrier mobility in strained silicon and reduced parasitic capacitance in SOI to form the SSOI.
- Strained silicon is first grown on relaxed SiGe and then transferred to a silicon wafer by direct wafer bonding.